Notice of Allowability	Application No.	Applicant(s)	
	10/813,267	IOVIN ET AL.	
	Examiner	Art Unit	
	Bryce P. Bonzo	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Application as filed*.

2. ☒ The allowed claim(s) is/are *1-24*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER

Reasons for Allowance

Claims 1-24 are allowed. Below is the reasoning for this indication of allowable subject matter. Applicant is reminded the claims are allowed as a whole, and any modification to the claims may result in a removal of allowability.

Claims 1-6 contain the following features in combination:

1. A debugging system comprising:

a host system to observe and control *the step-by-step execution of a debugging operation*;

a target system communicatively coupled to the host system, the target system including

a debug port having a plurality of pins;

a debug port interface coupled to the debug port; and

a power management pin separate from said plurality of pins and not coupled to the debug port via the debug port interface; and

a connection to couple one of said plurality of pins to said power management pin, said connection being independent of said debug port interface.

The cited prior art does not describe the particular arrangement of pins of a debug port and connections to the power management pin as shown above.

Claims 7-9 and 16-18 contain the following features in combination:

7. A method of debugging, comprising:

sampling a power management signal on a device, the power management signal being separate from a test access port of the device;

determining whether a power management transition has occurred on the *based on the power management signal*; and

triggering a *debug mode if a power management transition* has occurred.

The cited prior art does not describe the use of management signals. The prior art's closest comparable technology checks error status signals at power up, but does not initiate debugging on the management signals accord.

Claims 10-12 and 19-21 contain the following features in combination:

10. A method of debugging, comprising:

issuing a command to halt execution on a device;

querying a sleep pin on the device to determine whether the sleep pin is asserted;

asserting a system error pin on the device to wake up the device;

querying a stopclock pin on the device to determine whether the sleep pin is de-asserted; and

processing the halt command.

The prior art does not make use of these three pins in this precise manner in debugging.

Claims 13-15 contain the following features in combination:

13. A method of debugging, comprising:

deferring power management transitions on a device;

issuing a test access port scan to the device; and

determining whether a power management transition occurred during the test access port scan.

The Examiner was unable to find any explicit teaching of how to handle power management transitions in the use of TAP scans. All literature on the subject ignores the power during a TAP scan.

22. A machine accessible medium containing program instructions that, when executed by a processor, cause the processor to:

receive a command that indicates to the processor how to defer power state transitions in a target device;

clear a first bit and a second bit in a designated register of a target device if the command indicates that power state transitions are not deferred;

set the first bit and clear the second bit if the command indicates that power state transitions are always deferred;

set the first bit and clear the second bit if the target device is in debug mode and the command indicates that power state transitions are deferred while the target device is in debug mode; and

clear the first bit and set the second bit if the target device is not in debug mode and the command indicates that power state transitions are deferred after a breakpoint.

As described above, the process of deferring debugging based on a power states was not found, these claims describe the specific memory mechanisms which provide for that deferring.